Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (Currently Amended) A data memory interface apparatus comprising:

at least one interface for transmitting data and receiving data at a first data rate;

at least one memory interface for transmitting data to and receiving data from at least one dual data rate memory at a second data rate;

at least one processing circuit for generating and receiving at least one dual edged data strobe to transmit data to and receive data from the at least one dual data rate memory[[.]];

wherein the at least one interface uses a clock operating at the second data rate and at least one phase reference signal to clock data into or out of the at least one interface; and

wherein the at least one phase reference signal is indicative of either rising edges or falling edges of a clock operating at the first data rate.

2. (Cancelled)

3. (Cancelled)

4. (Currently ameded) The apparatus of claim [[2]]1 wherein the at least one phase reference signal is distributed in a daisy chain to a plurality of processing modules in the at least one processing circuit.

5. (Original) The apparatus of claim 1 wherein the at least one interface comprises at least one register for clocking data into or out of the at least one interface according to a clock operating at the second data rate.

6. (Original) The apparatus of claim 1 wherein the at least one processing circuit comprises at least one delay lock loop for delaying the at least one dual-edged data strobe.

7. (Original) The apparatus of claim 6 wherein the at least one delay lock loop provides substantially equal delays for a 100 MHz dual-edged data strobe and a 133 MHz dual-edged data strobe.

8. (Original) The apparatus of claim 1 wherein the at least one processing circuit comprises at least one alternating inverting buffer tree for generating the at least one dual-edged data strobe.

9. (Original) The apparatus of claim 1 wherein the at least one processing circuit generates data according to a first edge of a clock operating at the second data rate and generates the at least one dual-edged data strobe according to a second edge of the clock that immediately follows the first edge.

10. (Original) The apparatus of claim 1 wherein the at least one processing circuit selectively gates the at least one dual-edged data strobe when receiving data from the at least one dual data rate memory.

11. (Original) The apparatus of claim 10 wherein the at least one dual-edged data strobe is gated off from at least a portion of the at least one processing circuit when the at least one dual-edged data strobe is in a high impedance state.

12. (Original) The apparatus of claim 1 wherein the at least one processing circuit comprises a plurality of processing modules for processing bytes of data transmitted to and received from the at least one dual data rate memory.

13. (Original) The apparatus of claim 1 wherein the at least one processing circuit comprises at least one data memory for storing data received from the at least one dual data rate memory.

14. (Original) The apparatus of claim 13 wherein the at least one data memory comprises at least one FIFO.

15. (Original) The apparatus of claim 1 wherein the at least one dual data rate memory comprises DDR SDRAM.

16. (Original) The apparatus of claim 1 wherein the at least one interface comprises at least one buffer.

17. (Original) A method of interfacing to a data memory comprising: transmitting data from and receiving data by at least one interface at a first data rate;

transmitting data to and receiving data from at least one dual data rate memory at a second data rate;

generating and receiving at least one dual edged data strobe to transmit data to and receive data from the at least one dual data rate memory[[.]]; and

clocking data into or out of the at least one interface using a clock operating at the second data rate and at least one phase reference signal;

wherein the at least one phase reference signal is indicative of either rising edges or falling edges of a clock operating at the first data rate.

18. (Cancelled)

19. (Cancelled)

20. (Currently amended) The method of claim [[18]]17 wherein the at least one phase reference signal is distributed in a daisy chain to a plurality of processing modules.

21. (Original) The method of claim 17 comprising delaying the at least one dual-edged data strobe by at least one delay lock loop.

22. (Original) The method of claim 21 wherein the at least one delay lock loop provides substantially equal delays for a 100 MHz dual-edged data strobe and a 133 MHz dual-edged data strobe.

23. (Original) The method of claim 17 comprising generating the at least one dual-edged data strobe by at least one alternating inverting buffer tree.

24. (Original) The method of claim 17 comprising generating data according to a first edge of a clock operating at the second data rate and generating the at least one dual-edged data strobe according to a second edge of the clock that immediately follows the first edge.

25. (Original) The method of claim 17 comprising selectively gating the at least one dual-edged data strobe when receiving data from the at least one dual data rate memory.

26. (Original) The method of claim 25 wherein the at least one dual-edged data strobe is gated off when the at least one dual-edged data strobe is in a high impedance state.

27 (Currently amended) A data memory interface apparatus comprising:

at least one interface for transmitting data to and receiving data from ~~the~~ at least one data processor at a first data rate using a clock signal operating at a second data rate and a phase reference signal;

at least one memory interface for transmitting data to and receiving data from at least one DDR SDRAM at a second data rate according to at least one DQS signal;

at least one FIFO for storing data received from the at least one DDR SDRAM; and

at least one processing circuit comprising:

at least one circuit for selectively gating at least one DQS signal received from the at least one DDR SDRAM;

at least one delay lock loop for delaying at least one DQS signal received from the at least one DDR SDRAM; and

at least one alternating inverting buffer tree for generating a plurality of DQS signals from the delayed at least one DQS signal to clock data into the at least one FIFO[[.]];

wherein the at least one phase reference signal is indicative of either rising edges or falling edges of a clock operating at the first data rate.

28. (Cancelled)

29. (Original) The apparatus of claim 27 wherein the at least one phase reference signal is distributed in a daisy chain to a plurality of processing modules in the at least one processing circuit.

30. (Original) The apparatus of claim 27 wherein the at least one processing circuit generates data according to a first edge of a clock operating at the second data rate and generates the at least one DQS signal according to a second edge of the clock that immediately follows the first edge.

31. (Original) The apparatus of claim 27 wherein the at least one DQS signal is gated off from at least a portion of the at least one processing circuit when the at least one dual-edged data strobe is in a high impedance state.

32. (Original) The apparatus of claim 27 wherein the at least one processing circuit comprises a plurality of processing modules for processing bytes of data transmitted to and received from the at least one DDR SDRAM.